Integrally gated carbon nanotube-on-post field emitter arrays

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Multiwalled carbon nanotubes were grown using chemical vapor deposition on the tops of blunt vertical silicon posts in cells having a horizontal gate aperture of conventional field emitter design. We obtained over 1 mA total emission current from a single array, or 0.3 μA per cell at 40 V. In addition to the low voltage operation, the most distinctive differences from conventional field emitter arrays include their stability and the lack of catastrophic arcing without any special sample preparation. [DOI: 10.1063/1.1428775]

Carbon nanotubes (cNT) are excellent field emitters on account of their chemical, structural, and electronic properties, which afford important aspects of robustness that have been lacking in the conventional metal and silicon field emitter arrays (FEA). They possess high current-carrying capacity and mechanical strength. Their small diameters (2–50 nm) and high aspect ratios produce high geometric field enhancement, which remains nearly constant even when material is removed from the end of the tubes such as by back ion bombardment. A key contributing factor to their stability as field emitters is the lack of surface oxide formation. Surface oxide formation on metal or silicon emitters impedes electron transport to the surface and causes changes in the emission characteristics during operation. Furthermore, the oxides could be the main cause for FEA catastrophic destruction by trapping charge which could lead to arcing.[1] It has also been suggested that carbon nanotubes do not form nanoprotrusions as metal and silicon cathodes do, thus making current runaway and arcing less likely to occur.[2]

Numerous works have been published on cNT emitters in a diode configuration in which the cNTs, either grown or placed as dense mats on substrates, were placed at a known separation from an anode. Very low turn-on electric fields (as low as 1–2 V per micron), high currents from single tubes (over 1 μA)[3] and long term stability have been reported.[2] Because the cNT–anode separations were usually many microns, the voltages used were usually too large for most applications. Fabrication of the nanotubes within microfabriated gates can reduce the required voltage and enable more control of small arrays such as the pixels in flat panel displays. Other applications requiring integral gates include high frequency amplifiers, spacecraft propulsion systems, high voltage, and high temperature electronics, portable x-ray sources, multibeam electron beam lithography, etc.

To date only a few works on gated cNT emitters have been published, and they took two general approaches; using (1) a cNT paste (cNT mixed in a binding matrix) technology,[4–8] or (2) *in situ* chemical vapor deposition (CVD) growth of cNT. With the exception of the work of Wang and co-workers,[8] the earlier efforts using the first approach, in conjunction with screen printing and the construction of ''grid gates,''[4] ''undergates,''[5,6] or ''normal gates,''[7] still require relatively high voltages (threshold over 70 V).

To date three reports on gated *in situ* grown cNT FEAs with demonstrated emission have been published: (1) Lee and co-workers[9] have grown cNTs inside open gated apertures. (2) Our group has grown cNTs on tops of gated silicon posts as well as inside open gated apertures.[10,11] (3) Ahn and co-workers have grown cNTs inside open trenches with a buried gate.[12] The scarcity of reports on the *in situ* growth approach is largely due to the difficulty of controlling the growth of cNTs (both in length and direction) as well as maintaining structural integrity at the growth temperature.

Growing cNTs on top of tall gated post structures allows the use of relatively short cNTs. Longer tubes grown from the bottoms of open holes are flexible, thus it is difficult to control the tip positions relative to the gate apertures. Placing short emitters on top of tall posts improves control, and thus reduces the probability of shorting by cNTs bridging to the gate. Such structures also allow thick gate insulators, important in high frequency applications.

We used arrays of gated silicon posts as starting structures; one unit cell is illustrated in Fig. 1. The structures were fabricated at MCNC using a slight variation of the well documented method[13,14] for fabricating the silicon tip-on-post FEAs. The silicon tips in the particular arrays used here were relatively blunt. The silicon posts are about 2 μm high and 1 μm in diameter. The Cr gates are 0.45 μm thick and have 2.5 μm diameter apertures with 4 μm spacing. Both cathode and gate contact pads are incorporated on the top of the substrate for each array. Each growth substrate contained many arrays, electrically isolated from each other.

The cNT growth process began with sputter deposition of a thin film of Ni ($<$20 nm) onto the starting substrate. The substrate was then dipped in buffered HF to liftoff Ni from the oxide areas (cell sidewalls and oxide regions separating arrays). After rinsing in distilled water and drying, the sample was placed in a coldwall, hot-filament assisted CVD reactor on top of a 2.5 cm diameter Mo heater concentrically placed within the reactor tube, with the flow of gases perpendicular to the sample substrate. The hot filament consisted of a W ribbon 25 μm thick and 2 mm wide, positioned about 1

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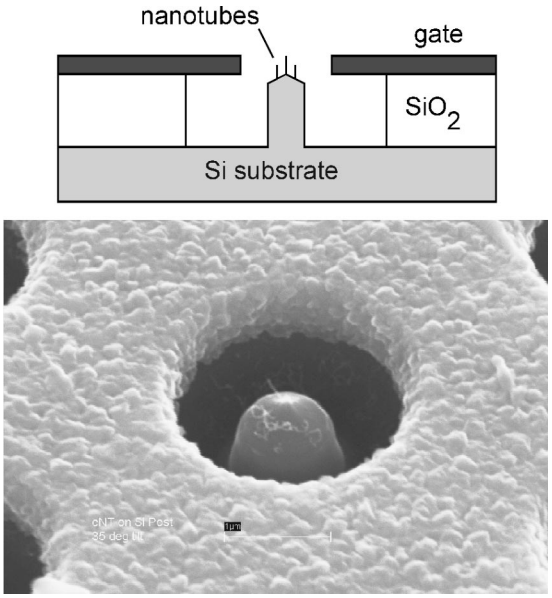

FIG. 1. Gated carbon nanotubes-on-silicon post field emitter cell. Top: schematic drawing of cell; bottom: scanning electron micrograph of cell with multiwalled carbon nanotubes on a silicon post centered in a 2.5 μm diameter chrome gate aperture.

cm above and parallel to the heater surface. A typical growth run began by heating in flowing argon, followed by replacing argon with ammonia gas at a flow of 80 sccm, turning on the hot filament (to 1900 °C), and after 3–5 min, admitting ethylene or acetylene gas at 20 sccm into the reactor. The equilibrium growth temperatures were 650–700 °C and the reactor pressures were 21–24 Torr. Growth duration ranged from 0.5 to 4.5 min.

The sample top surface proved to be relatively free not only of cNTs but also of amorphous carbon, which is necessary so as not to have neighboring arrays be shorted together. No cNT grew on the chrome gate because Ni (in quantity as deposited) apparently diffused into or alloyed with chrome at the high growth temperatures, thereby losing catalytic activity for cNT growth. No significant amorphous carbon could build up due to the excess ammonia (likely ammonia-derived radicals such as H, NH_2, and NH which reacted with carbon). Using a SEM, we observed nanotubes (with 20–30 nm diameters indicating multiwalled cNT growth) on the Si posts and sometimes inside the FEA cells as well. The latter was due to the incomplete removal of Ni from the cell sidewalls. We believe that cNTs bridging the substrate and the gate inside the cell caused some gate leakage current. We anticipate that optimizing the fabrication process can reduce the leakage current.

The lower panel in Fig. 1 shows a SEM image of one cell from an array with cNTs grown on top of the Si post. This particular array had 37 000 cells of which only about 5%–10% (from SEM examination) of the Si posts had cNTs. Apparently much Ni could haave reacted with Si at the growth temperatutre or it could have been either removed or deactivated by HF from the tops of most of the Si posts (which might not have been entirely free of oxide after a removal pretreatment). However, among a number of working samples we have fabricated, this array has produced the highest current so far obtained, a maximum current of 1.1 mA at a gate voltage of 41 V. Assuming 10% of the cells had

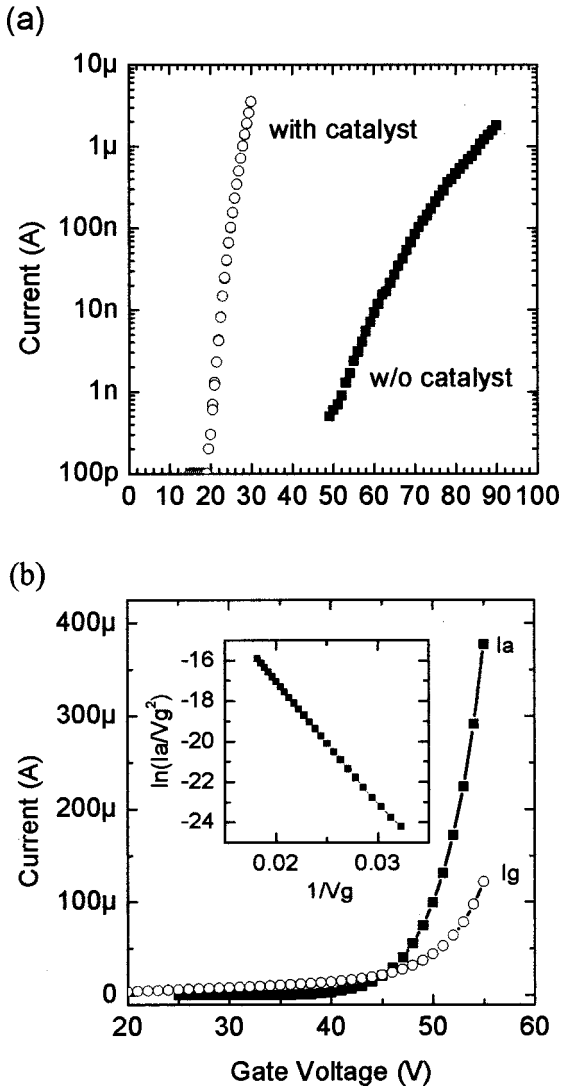

FIG. 2. Emission current–voltage characteristics from arrays of cNT-on-silicon post-FEAs. (a) Anode current vs gate voltage plots for arrays with and without cNTs. (b) Anode current (filled squares) and gate current (open circles) vs gate voltage plot and corresponding Fowler–Nordheim plot of the anode current from an array of 37 000 cells.

cNTs, this current corresponded to about 300 nA per cell.

Emission characterization was carried out in an UHV chamber (base pressure 10^{-10} Torr) equipped with an ion pumped load lock, sample stage heater, and quadrupole mass analyzer. We outgassed the arrays in UHV at a maximum temperature of 600 °C to remove most of the adsorbed molecules. In addition to water and CO, acetylene fragments appeared in the residual gas spectrum as the array was heated. We used tungsten wire probes as an anode and to contact the cathode and gate. Computer-controlled electrometers acquired the emission data. The anode probe was placed at about 1 mm from the arrays at 200 V with respect to the cathode probe. Varying the anode potential ± 25 V did not change the gate or anode current.

Figure 2(a) shows comparison between $I-V$ curves of two arrays processed at the same time, but the Ni catalyst was omitted from one. As expected, the array without the catalyst had a much higher threshold voltage. The comparison showed that cNTs were responsible for reducing the gate voltage. The array processed with the catalyst showed a threshold voltage near 20 V.

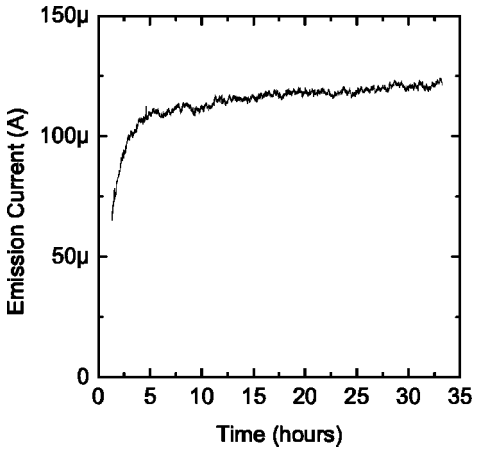

FIG. 3. Anode current–time plot of array operating at constant gate potential of 60 V during 32 h just after baking the array to 600 °C and cooling in UHV.

The voltage needed to produce a given current was typically lowest when the array was first turned on. The $I-V$ curves were stable and reproducible when the arrays were operated within a given range of gate voltage. Operating the array at a higher gate potential than previously seen shifted the $I-V$ curve to a higher voltage. Fowler–Nordheim plots of these data were linear and parallel. We did not observe any damage to the gate after the $I-V$ curve shifted, as is often the case when metal or silicon emission sites are damaged. This behavior indicates that some of the nanotubes that emitted at the lowest gate voltages were altered during emission at higher currents. The altered state could be due to either a change in the geometry or the electronic properties of the affected nanotubes (the latter, for example, by desorption of adsorbates from the cNTs).

Current–voltage data obtained from an array (containing 37 000 apertures) after baking are shown in Fig. 2(b). A Fowler–Nordheim plot of the same data (inset) shows linear behavior. The gate current was dominated by leakage below 45 V, but tracked the anode current (~30% anode current) at higher voltages.

Figure 3 shows an anode current–time plot for an array soon after cooling from 600 °C in UHV. The short-term noise was less than 5%. The emission current increased substantially during the first few hours and continued to increase slowly during the rest of the 32 h period. The increase in current may be the result of adsorbed water vapor[2,3] from background ambient in the chamber. Deliberately exposing the arrays to water vapor also increased the emission current. Additional experiments on the effects of adsorbed molecules will be published separately.

Operating the arrays and gate voltages in excess of 40–60 V tended to increase the gate current over time. In cases where the gate current exceeded 1 mA, the gate was often damaged and shorted to the cathode. Thus the damage appeared to be due to the gate current rather than an emitter-gate arc, as can occur in arrays built with silicon and metal emitters. Optimization of the fabrication process to reduce the gate current should minimize that type of gate damage. We believe the relative stability and lack of arcing that we observed in the nanotube arrays can be attributed to the lack of a nonvolatile oxide, which might otherwise hinder emission as it can in silicon[1] and probably many other field emitters.

In conclusion, we reported the proof of principle of the fabrication of an *in situ* grown microgated cNT field emitter array. The initial results presented in this letter demonstrate emission at much lower voltages than previously obtained from field emitter arrays with similar dimensions. The low operating voltage, together with other properties of the nanotube emitters appear to be responsible for relatively robust operating characteristics.

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[1] J. Shaw, J. Vac. Sci. Technol. B **18**, 1817 (2000).
[2] K. A. Dean and B. R. Chalamala, Appl. Phys. Lett. **75**, 3017 (1999).
[3] K. A. Dean and B. R. Chalamala, Appl. Phys. Lett. **76**, 375 (2000).
[4] N. S. Lee, D. S. Chung, I. T. Han, J. H. Kang, Y. S. Choi, H. H. Kim, S. H. Park, Y. W. Jin, W. K. Yi, M. J. Yun, J. E. Jung, C. J. Lee, J. H. You, S. H. Jo, C. G. Lee, and J. M. Kim, Diamond Relat. Mater. **10**, 265 (2001).
[5] J. H. Kang, Y. S. Choi, W. B. Choi, N. S. Lee, Y. J. Park, J. H. Choi, H. Y. Kim, Y. J. Lee, D. S. Chung, Y. W. Jin, J. H. You, S. H. Jo, J. E. Jung, and J. M. Kim, Mater. Res. Soc. Symp. Proc. **621**, R5.2.1 (2000).
[6] S. H. Jo, K. W. Jung, Y. J. Kim, S. H. Ahn, J. H. Kang, H. S. Han, B. G. Lee, J. C. Cha, S. J. Lee, S. Y. Park, C. G. Lee, J. H. You, N. S. Lee, and J. M. Kim, *Proceedings of the 14th International Vacuum Microelectronics Conference* (IEEE, Davis, CA, 2001), pp. 31–32.
[7] J. W. Nam, Y. S. Jo, M. J. Yoon, H. Y. Kim, M. A. Yu, S. H. Cho, S. J. Lee, H. K. Park, K. S. Choi, J. H. You, N. S. Lee, and J. M. Kim, *Proceedings of the 14th International Vacuum Microelectronics Conference* (IEEE, Davis, CA, 2001), pp. 57–58.
[8] Q. H. Wang, M. Yan, and R. P. H. Chang, Appl. Phys. Lett. **78**, 1294 (2001).
[9] Y. H. Lee, Y. T. Jang, D. H. Kim, J. H. Ahn, and B. K. Ju, Adv. Mater. **13**, 479 (2001).
[10] D. S. Y. Hsu and J. L. Shaw, *Proceedings of the 14th International Vacuum Microelectronics Conference* (IEEE, Davis, CA, 2001), pp. 51–52.
[11] J. L. Shaw and D. S. Y. Hsu, *Proceedings of the 14th International Vacuum Microelectronics Conference* (IEEE, Davis, CA, 2001), pp. 45–46.
[12] S. D. Ahn, Y. H. Song, S. Y. Choi, J. B. Park, J. I. Sohn, S. H. Lee, J. H. Lee, and K. I. Cho, *Proceedings of the 14th International Vacuum Microelectronics Conference* (IEEE, Davis, CA, 2001), pp. 55–56.
[13] D. Temple, C. A. Ball, W. D. Palmer, L. N. Yadon, D. Vellenga, J. Mancusi, G. E. McGuire, and H. F. Gray, J. Vac. Sci. Technol. B **13**, 150 (1995).
[14] D. Palmer, H. F. Gray, J. Mancusi, D. Temple, C. Ball, J. L. Shaw, and G. E. McGuire, J. Vac. Sci. Technol. B **13**, 576 (1995).